Nikolaos Bellas

Associate Professor

December 2019

Department of Electrical and Computer Engineering

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Research Interests

Architecture of computing systems: reconfigurable systems; heterogeneous systems; embedded systems; reliable computing; approximate computing; low-power design; computer architecture;

Software: EDA tools for architectural synthesis; system software for reliable and approximate computing; multimedia

Employment History

04.2008 - now **Associate Professor.** ECE Department, University of Thessaly, Volos, Greece

09.2007-05.2008 **Industrial Consultant.** Ported the AVS video decoding standard to the Tensilica Diamond processor using Tensilica instruction extensions and dual core API.

10.2001-03.2007 **Principal Staff Engineer.** Embedded Systems Research., Motorola Inc., Schaumburg, IL. Technical lead of a five-person team working on reconfigurable computing.

Designed CAD tool that compiles streaming applications written in a high level language to accelerators in a System On FPGA platform.

Chief architect of two ASIC chips that perform image processing for wireless multimedia applications for the next generation camera-enabled Motorola phones. The image sensor companion chips are used to perform image processing, sensor control, color space conversion, etc.

Participated in the design of a System On Chip ASIC design for an automotive application. The chip was based on the ARM9 RISC processor and a streaming co-processor to accelerate performance critical kernels. Developer of a cycle accurate simulator of the co- processor to be used for chip functional verification.

05.1999-10.2001 **Senior Staff Engineer.** Multimedia Architecture Lab, Motorola Inc., Schaumburg, IL

Architect of a scalable, programmable architecture for MPEG4 video and JPEG image compression.

Designed a programmable Motion Estimation module and defined an Instruction Set Architecture for motion estimation algorithms.
Designed the image-processing module that interfaces to the image sensor and wrote a bit-exact functional model for the MPEG4 encoder for chip verification.

Participated in chip hardware testing, and in the design and implementation of the image processing algorithms. The chip is used in Motorola's first 3G (Third Generation) camera cell phone

12.1998-05.1999 **Postdoctoral research associate,** Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Champaign, IL

05.1996-08.1996 **Research Intern.** Design Technology Labs, Intel Corp., Santa Clara, CA

05.1995-08.1995 **Research Intern**. Silicon Graphics (SGI), Mountain View, CA

08.1993-12.1998 **Graduate Research Assistant.** Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Champaign, IL

Education

1998 **PhD.** Electrical and Computer Engineering, University of Illinois at Urbana-Champaign.
Dissertation Title: "*Architectural and Compiler Support for Energy Reduction in High Performance Microprocessors*".
Advisors: Ibrahim Hajj and Constantine Polychronopoulos
GPA: 5.0/5.0

1995 **MSc.** Electrical and Computer Engineering, University of Illinois at Urbana-Champaign.
Thesis Title: "*A Novel Design for Testability Technique Using State Space Information*"
Advisor: Daniel Saab.
GPA: 5.0/5.0

1992 **Diploma**. Computer Engineering and Informatics. University of Patras, Greece
GPA: 9.15/10

Peer Reviewed Publications

Journal Articles

J11. Konstantinos Parasyris, Vassilis Vassiliadis, Christos D Antonopoulos, Spyros Lalis, Nikolaos Bellas. Significance-Aware Program Execution on Unreliable Hardware. *ACM Transactions on Architecture and Code Optimization (TACO).* Vol. 14 (2). April 2017.

J10. Vassilis Vassiliadis, Charalampos Chalios, Konstantinos Parasyris, Christos D. Antonopoulos, Spyros Lalis, Nikolaos Bellas, Hans Vandierendonck, Dimitrios S. Nikolopoulos. Exploiting Significance of Computations for Energy-Constrained Approximate Computing. *International Journal of Parallel Programming (IJPP).* pg. 1078-1098. March 2016.

J9. K. Krommydas, Wu-chun Feng, Christos D. Antonopoulos, and N. Bellas. OpenDwarfs: Characterization of Dwarf-Based Benchmarks on Fixed and Reconfigurable Architectures. *Journal of Signal Processing Systems.* US Springer, 85(3), pg. 373-392. 2016.

J8. M. Owaida, G. Falcao, J. Andrade, C. Antonopoulos, N. Bellas, M. Purnaprajna, D. Novo, G. Karakonstantis, A. Burg, and P. Ienne. Enhancing design space exploration by extending CPU/GPU specifications onto FPGAs. *ACM Transactions on Embedded Computing Systems (TECS).* Vol 14(2). March 2015.

J7. Dimitrios Nikolopoulos, Hans Vandierendock, Nikolaos Bellas, Christos D. Antonopoulos, Spyros Lalis, Georgios Karakonstantis, Andreas Burg, Uwe Naumann. Energy Efficiency through Significance-Based Computing. *IEEE Computer*. Vol. 47. Issue 7. Pg. 82-85. July 2014.

J6. Maria Koziri, Dimitris Zacharis, Ioannis Katsavounidis, Nikolaos Bellas. Implementation of the AVS Video Decoder on a Heterogeneous Dual-Core SIMD Processor. *IEEE Transactions on Consumer Electronics*, vol. 57, No. 2, pp. 673-681, May 2011.

J5. Seda Ogrenci Memik, Nikolaos Bellas, Somsubhra Mondal. Pre-synthesis Area Estimation of Reconfigurable Streaming Accelerators. *IEEE Transactions on Computer-Aided Design*, Volume: 27, No: 11, pp. 2027-2038, November 2008.

J4. Nikolaos Bellas, Sek Chai, Malcolm Dwyer, Dan Linzmeier. Mapping streaming architectures on reconfigurable platforms. *ACM SIGARCH Computer Architecture News.* Volume 35, Issue 3, Pages: 2 – 8, June 2007

J3. Nikolaos Bellas, Ibrahim Hajj, Constantine Polychronopoulos. Using dynamic cache management techniques to reduce energy in general purpose Processors. *IEEE Transactions on VLSI Systems*, Volume: 8, Issue : 6, pp. 693-708, December 2000.

J2. Nikolaos Bellas, Ibrahim Hajj, Constantine Polychronopoulos, George Stamoulis. Architectural and Compiler Techniques for Energy Reduction in High Performance Microprocessors. *IEEE Transactions on VLSI Systems, Special Issue on Low Power,* Volume:8, Issue:3, pp. 317-326, June 2000

J1. Amber-Roy Chowdhury, Nikolaos Bellas, Prithviraj Banerjee. Algorithm Based Error Detection Schemes for Iterative Solution of Partial Differential Equations. *IEEE Transactions on Computers*, pp. 394-407, Vol. 45, Number 4, April 1996

Conference and Workshop Articles

C46. Christos Kalogirou, Panos Koutsovasilis, Christos D. Antonopoulos, Nikolaos Bellas, Spyros Lalis, Srikumar Venugopal and Christian Pinto. Exploiting CPU Voltage Margins to Increase the Profit of Cloud Infrastructure Providers. *19th IEEE/ACM International Symposium on Cluster, Cloud and Grid Computing, (CCGrid).* May 14-17, 2019. Larnaca, Cyprus.

C45. Maria Rafaela Gkeka, Nikolaos Bellas, Christos D. Antonopoulos. Comparative Performance Analysis of Vulkan Implementations of Computational Applications. *7th International Workshop on OpenCL (IWOCL).* May 13-15, 2019. Boston, MA.

C44. K. Parasyris, N. Bellas, C. D. Antonopoulos, and S. Lalis. Exploring the Effects of Code Optimizations on CPU Frequency Margins. *Workshop in Approximate and Transprecision Computing on Emerging Technologies (ATCET), in conjunction with the International Supercomputing Conference (ISC).* June 28th, 2018. Frankfurt, Germany.

C43. K. Parasyris, P. Koutsovasilis, V. Vassiliadis, Christos D. Antonopoulos, Nikolaos Bellas, Spyros Lalis. A Framework for Evaluating Software on Reduced Margins Hardware. *International Conference on Dependable Systems and Networks (DSN).* June 25-28, 2018. Luxemburg.

C42. Georgios Karakonstantis et al. An Energy-Efficient and Error-Resilient Server Ecosystem Exceeding Conservative Scaling Limits. *IEEE Conference on Design, Automation and Test in Europe (DATE).* March 2018. Dresden, Germany.

C41. Christos Kalogirou, Panos Koutsovasilis, Manolis Maroudas, Christos D. Antonopoulos, Spyros Lalis, Nikolaos Bellas. Edge and Cloud Provider Cost Minimization by Exploiting Extended Voltage and Frequency Margins. *International Conference on Parallel Computing (PARCO),* September 12-15, 2017, Bologna, Italy

C40. Ioannis Parnassos, Nikolaos Bellas, Nikolaos Katsaros, Nikolaos Patsiatzis, Athanasios Gkaras, Konstantinos Kanellis, Christos D. Antonopoulos, Michalis Spyrou, Manolis Maroudas. Programming Model and Runtime System for Approximation-Aware Heterogeneous Computing. *27th International*

Symposium on Field Programmable Logic and Applications (FPL). September 4-8, 2017. Ghent, Belgium (short paper)

C39. Ioannis Parnassos, Panagiotis Skrimponis, Georgios Zindros, Nikolaos Bellas. SoCLog: A Real-Time, Automatically Generated Logging and Profiling Mechanism for FPGA-based Systems On Chip. *26th International Symposium on Field Programmable Logic and Applications (FPL).* August 28 – September 2, 2016. Lausanne, Switzerland (short paper)

C38. Vassilis Vassiliadis, Jan Riehme, Jens Deussen, Konstantinos Parasyris, Christos D. Antonopoulos, Nikolaos Bellas, Spyros Lalis and Uwe Naumann. Towards Automatic Significance Analysis for Approximate Computing. *International Symposium on Code Generation and Optimization (CGO).* March 14-16, 2016. Barcelona, Spain.

C37. Michalis Spyrou, Christos Kalogirou, Christos Konstantas, Panos K. Koutsovasilis, Manolis Maroudas, Christos D. Antonopoulos, Nikolaos Bellas. Energy Minimization on Heterogeneous Systems through Approximate Computing. *International Conference on Parallel Computing (PARCO),* September 1-4, 2015. Edinburgh, UK.

C36. Vassilis Vassiliadis, Charalampos Chalios, Konstantinos Parasyris, Christos D. Antonopoulos, Spyros Lalis, Nikolaos Bellas, Hans Vandierendonck, Dimitrios S. Nikolopoulos. A Significance-Driven Programming Framework for Energy-Constrained Approximate Computing. *ACM International Conference on Computing Frontiers.* May 18-21, 2015. Ischia, Italy.

C35. Konstantinos Parasyris, Vassilis Vassiliadis, Christos D. Antonopoulos, Spyros Lalis and Nikolaos Bellas. A Significance-Aware Software Stack for Computing on Unreliable Hardware. *Second Workshop on Approximate Computing Across the System Stack (WACAS).* March 15, 2015. Istanbul, Turkey.

C34. Vassilis Vassiliadis, Konstantinos Parasyris, Charalampos Chalios, Christos D. Antonopoulos, Spyros Lalis, Nikolaos Bellas, Hans Vandierendonck, Dimitrios S. Nikolopoulos. A programming model and runtime system for significance-aware energy-efficient computing. *ACM SIGPLAN 20th Symposium on Principles and Practice of Parallel Programming (PPoPP*). February 9-11, 2015. San Francisco, CA (short paper)

C33. Konstantinos Parasyris, Georgios Tziantzioulis, C.D. Antonopoulos, Nikolaos Bellas. GemFI: A Fault Injection Tool for Studying the Behavior of Applications on Unreliable Substrates. *International Conference on Dependable Systems and Networks (DSN).* June 23-26, 2014. Atlanta, GA

C32. Konstantinos Krommydas, Wu-Chun Feng, Muhsen Owaida, Christos D. Antonopoulos and Nikolaos Bellas. On the Portability of OpenCL Dwarfs on Fixed and Reconfigurable Parallel Platforms. *25th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP).* June 18-20, 2014, Zurich, Switzerland. **(Nominated for Best Paper Award).**

C31. Muhsen Owaida, Christos D. Antonopoulos, Nikolaos Bellas. A Grammar Induction Method for Clustering of Operations in Complex FPGA Designs. *IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM), Regular paper.* May 11-13, 2014. Boston, MA

C30. Gabriel Falcao, Muhsen Owaida, David Novo, Madhura Purnaprajna, Nikolaos Bellas, Christos D. Antonopoulos, Georgios Karakonstantis, Andreas Burg and Paolo Ienne. Shortening design time through multiplatform simulations with a portable OpenCL golden-model: the LDPC decoder case. *IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)*, April-May 2012. Toronto, ON.

C29. Muhsen Owaida, Nikolaos Bellas, Christos Antonopoulos, Konstantis Daloukas, Charalambos Antoniadis. Massively Parallel Programing Models Used as Hardware Description Languages: The OpenCL Case. *International Conference on Computer-Aided Design (ICCAD),* November 6-10, 2011, San Jose, CA

C28. Konstantinos Krommydas, Wu-Chun Feng, Christos Antonopoulos, Nikolaos Bellas. AVS Video Decoder on Multicore Systems: Optimizations and Tradeoffs. *In Proceedings of the 2011 International Conference on Multimedia and Expo (ICME) – Industrial Program*, July 2011, Barcelona, Spain

C27. Georgios Karakonstantis, C.D. Antonopoulos, Nikolaos Bellas, Kaushik Roy. Significance Driven Computation on Next Generation Unreliable Platforms. *Design Automation Conference (DAC), Wild And Crazy Ideas Session (WACI)*, June 5-10, 2011, San Diego, CA

C26. Muhsen Owaida, Nikolaos Bellas, Konstantis Daloukas, Christos D Antonopoulos. Synthesis of Platform Architectures from OpenCL Programs. *IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)*, May 1-3, 2011, Salt Lake City, UT **(Highest number of citations in FCCM 2011).**

C25. Kostas Theocharoulis, Haralambos Antoniadis, Nikolaos Bellas, C.D. Antonopoulos. Implementation and Performance Analysis of Seal Encryption on FPGA, GPU, and Multicore Processors. *IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)*, May 1-3, 2011, Salt Lake City, UT (short paper)

C24. Muhsen Owaida, Christos D Antonopoulos, Nikolaos Bellas, Konstantis Daloukas, Charalambos Antoniadis, Konstantinos Krommidas, Georgios Tsoublekas. Implementation and Performance Comparison of the Motion Compensation Kernel of the AVS Video Decoder on FPGA, GPU and Multicore Processors. *IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)*, May 1-3, 2011, Salt Lake City, UT (short paper)

C23. Konstantis Daloukas, C.D. Antonopoulos, Nikolaos Bellas. GLOpenCL: OpenCL Support on Hardware- and Software-Managed Cache Multicores. *6th International Conference on High Performance Embedded Architectures & Compilers (HiPEAC).* January 24-26, 2011, Heraklion, Greece.

C22. Konstantinos Krommidas, Georgios Tsoublekas, C.D. Antonopoulos, Nikolaos Bellas. Mapping and Optimization of the AVS Video Decoder on a High Performance Chip Multiprocessor. *International Conference on Multimedia and Expo (ICME)*, July 19-23, 2010, Singapore.

C21. Konstantis Daloukas, C.D. Antonopoulos, Nikolaos Bellas, Sek M. Chai. Fisheye Lens Distortion Correction on Multicore and Hardware Accelerator Platforms. 24th *International Parallel and Distributed Processing Symposium (IPDPS), A*pril 19-23, 2010, Atlanta, GA

C20. Nikolaos Bellas, Sek M. Chai, Malcolm Dwyer, Dan Linzmeier, Abelardo Lopez Lagunas. Proteus: An Architectural Synthesis Tool based on the Streaming Programing Model. *19th International Conference on Field Programmable Logic and Applications (FPL)*, August/September 2009, Prague, The Czech Republic (short paper)

C19. Sek M. Chai, Nikolaos Bellas, Abelardo Lopez Lagunas. Extending a Stream Programming Paradigm to Hardware Accelerator Platforms. *Symposium on Application Accelerators for High Performance Computing (SAAHPC 2009)*, July 27-31 2009, Champaign, IL

C18. Nikolaos Bellas, Ioannis Katsavounidis, Maria Koziri, Dimitris Zacharis. Mapping the AVS Video Decoder on a Heterogeneous Dual-Core SIMD Processor. *46th Design Automation Conference (DAC)-User Track*. July 26-31, 2009, San Francisco, CA

C17. Konstantis Daloukas, C.D. Antonopoulos, Nikolaos Bellas. Implementation of a Wide-angle Lens Distortion Correction Algorithm on the Cell Broadband Engine. 23rd *International Conference on Supercomputing (ICS)*, June 8-12, 2009, New York Metro Area, NY

C16. Nikolaos Bellas, Sek Chai, Malcolm Dwyer, Dan Linzmeier. Real-Time Fisheye Lens Distortion Correction Using Automatically Generated Streaming Accelerators. *IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)*, April 5-7, 2009, Napa Valley, CA

C15. Nikolaos Bellas, Sek Chai, Malcolm Dwyer, Dan Linzmeier. An Architectural Framework for Automated Streaming Kernel Selection. 14th *Reconfigurable Architectures Workshop (RAW)*, March 2007, Long Beach, CA

C14. Nikolaos Bellas, Sek Chai, Malcolm Dwyer, Dan Linzmeier. Mapping Streaming Architectures on Reconfigurable Platforms. *Reconfigurable and Adaptive Architectures Workshop (RAAW), in conjunction with Micro*, December 10th, 2006, Orlando, FL

C13. Somsubhra Mondal, Seda O. Memik, Nikolaos Bellas. Pre-synthesis area estimation of reconfigurable streaming accelerators. *16th International Conference on Field Programmable Logic and Applications (FPL)*, August 28-30 2006, Madrid, Spain (short paper)

C12. Nikolaos Bellas, Arnold Yanof. An Image Processing Pipeline with Digital Compensation of Low Cost Optics for Mobile Telephony. *International Conference on Multimedia and Expo (ICME)*, July 9-12, 2006, Toronto, Canada (short paper)

C11. Chai, Nikolaos Bellas, Greg Kujawa, Tom Ziomek, Linda Dawson, Tony Scaminaci, Malcolm Dwyer, Dan Linzmeier. Reconfigurable Streaming Architectures for Embedded Smart Camera Applications. *2nd IEEE Workshop on Embedded Computer Vision, in conjunction with CVPR*, June 18, 2006, New York, NY

C10. Nikolaos Bellas, Sek Chai, Malcolm Dwyer, Dan Linzmeier. FPGA implementation of a license plate recognition SoC using automatically generated streaming accelerators. 13th *Reconfigurable Architectures Workshop (RAW)*, 25-26 April 2006, Rhodes, Greece

C9. Nikolaos Bellas, Sek M. Chai, Malcolm Dwyer, Dan Linzmeier. Template-based generation of streaming accelerators from a high level representation. *International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, April 24-26, 2006, Napa Valley, CA (short paper)

C8. Somsubhra Mondal, Seda O. Memik, Nikolaos Bellas. Pre-synthesis Queue Size Estimation of Streaming Data Flow Graphs. *International Symposium on Field-Programmable Custom Computing Machines (FCCM)*, April 24-26, 2006, Napa Valley, CA (short paper)

C7. Sek Chai, Nikolaos Bellas, Malcolm Dwyer, Dan Linzmeier. Stream Memory Subsystem in Reconfigurable Platforms. 2nd *Workshop on Architecture Research using FPGA Platforms (WARFP)*, February 12, 2006, Austin, TX

C6. Nikolaos Bellas, Malcolm Dwyer. A programmable, high performance Vector array unit used for Real-time Motion Estimation. *Proceedings of the International Conference on Multimedia and Expo (ICME)*, Volume: 1, pp.117-120, July 2003, Baltimore, MD (short paper)

C5. Nikolaos Bellas, Ibrahim Hajj, Constantine Polychronopoulos, George Stamoulis. Energy and Performa Improvements in Microprocessor Design using a Loop Cache. *Proceedings of the International Symposium on Computer Design (ICCD)*, pp. 378-383, October 1999, Austin, TX

C4. Nikolaos Bellas, Ibrahim Hajj, Constantine Polychronopoulos. Using dynamic cache management techniques to reduce energy in a high-performance microprocessor. *International Symposium of Low Power Electronics and Design (ISLPED)*, pp. 64-69, August 1999, San Diego, CA

C3. Nikolaos Bellas, Ibrahim Hajj, Constantine Polychronopoulos. A detailed, transistor-level energy model for SRAM-based caches. *International Symposium of Circuits and Systems (ISCAS)*, Volume:6, pp.198-201, June 1999, Orlando, FL

C2. Nikolaos Bellas, Ibrahim Hajj, Constantine Polychronopoulos, George Stamoulis. Architectural and Compiler Support for Energy Reduction in the Memory Hierarchy of High Performance Microprocessors. *Proceedings of the International Symposium of Low Power Electronics and Design (ISLPED*), pp. 70-75, August 1998, Monterey, CA **(Highest number of citations in ISLPED 1998).**

C1. Nikolaos Bellas, Ibrahim Hajj, Constantine Polychronopoulos, George Stamoulis. A new scheme for I-Cache energy reduction in High Performance Processors. *Power-Driven Microarchitecture Workshop, International Symposium On Computer Architecture (ISCA),* June 1998, Barcelona, Spain

Patents

P13. **US Patent 8,855,441.** Sek M. Chai, Malcolm Dwyer, Dan Linzmeier, Ruei-Sung Lin, Nikolas Bellas. "Method and apparatus for transforming a non-linear lens-distorted image", October 2014, Motorola Corp.

P12. **US Patent 8,326,077.** Sek M. Chai, Malcolm Dwyer, Dan Linzmeier, Ruei-Sung Lin, Nikos Bellas. "Method and apparatus for transforming a non-linear lens-distorted image", December 2012, Motorola Corp.

P11. **US Patent 7,802,005.** Sek M. Chai, Nikos Bellas, Malcolm Dwyer, Dan Linzmeier. "Method and apparatus for configuring buffers for streaming data transfer". September 2010, Motorola Corp.

P10. **US Patent 7,683,948.** Arnold Yanof, Nikos Bellas. "System and method for bad pixel replacement in image processing". March 2010, Freescale Corp.

P9. **US Patent 7,603,492.** Sek M. Chai, Nikos Bellas, Malcolm Dwyer, Erica Lau, Zhiyuan Li, Dan Linzmeier. "Automatic generation of streaming data interface circuit", October 2009, Motorola Corp.

P8. **US Patent 7,580,070.** Arnold Yanof, Nikos Bellas**.** "System and method for roll-off correction in image processing", August 2009, Freescale Corp.

P7. **US Patent 7,441,224.** Nikos Bellas, Sek M. Chai, Dan Linzmeier. "Streaming kernel selection for reconfigurable processor", October 2008, Motorola Corp.

P6. **US Patent 7,305,649.** Nikos Bellas, Sek Chai, Erica Lau, Zhiyuan Li, Dan Linzmeier. "Automatic generation of streaming processor circuit", December 2007, Motorola Corp.

P5. **US Patent 7,073,041**. Malcolm Dwyer, Nikolaos Bellas. "Virtual Memory Translation Unit for Media Acceleration", July 2006, Motorola Corp.

P4. **US Patent 6,868,123.** Nikolaos Bellas, Malcolm Dwyer. "A programmable, high performance Vector array unit used for Real-time Motion Estimation", March 2005, Motorola Corp.

Patent Applications

P3. **US Patent Application 2006/0159339.** Sek M. Chai, Mohamed Ahmed, Nikos Bellas, Greg Kujawa, King F. Lee, Abelardo Lopez Lagunas. "Method and apparatus as pertains to captured image statistics ".

P2. **US Patent Application 2006/0262140.** Greg Kujawa, Mohamed Ahmed, Nikos Bellas, Sek M. Chai, King F. Lee, Abelardo Lopez Lagunas. "Method and apparatus to facilitate visual augmentation of perceived reality".

P1. **US Patent Application 2008/0120497.** Sek M. Chai, Nikos Bellas, Malcolm Dwyer, Dan Linzmeier. "Automated configuration of a processing system using decoupled memory access and computation"

Invited Talks, Panels, Tutorials

07.2017 Reliability and Energy-efficiency using Significance-Based Computing. Invited Talk at Design Test Verification and EDA Workshop. Volos, Greece.

02.2017 Reliability and Energy-efficiency optimizations using Significance-Based Computing. Invited Talk at Stanford Research Institute (SRI), Princeton, NJ.

10.2016 Reconfigurable Computing. Invited Talk at the University of Thessaly IEEE Student Branch.

09.2016 Approximate computing for next generation platforms. Talk ARM Research Summit. Cambridge, UK.

04.2016 A Benchmark Suite at the Meeting Point of Heterogeneous and Approximate Computing. Invited Talk at the Workshop on Benchmarking and Measuring Approximate Computing (BMAC) held in conjunction with ISPASS 2016. Uppsala, Sweden.

03.2016 Reliability and Energy-efficiency optimizations using Significance-Based Computing. Keynote Talk in Workshop on Parallel Programming for Resilience and Energy Efficiency (PP4REE). Barcelona, Spain.

03.2015 Enablers and Roadblocks for Mainstream Adoption of Approximate Computing Paradigm. Panel at WACAS 2015 in conjunction with ASPLOS 2015. Istanbul, Turkey.

10.2014 Significance-Based Computing for Reliability and Power Optimization. Invited Talk at HiPEAC Computing Systems Week. Athens, Greece.

09.2014 Significance-Based Computing for Reliability and Power Optimization. Invited Talk at the 6th International Conference on Numerical Analysis. Chania, Greece.

06.2014 Significance-Based Computing for Reliability and Power Optimization. Invited Talk at the Department of Informatics and Telecommunications, University of Athens, Greece

05.2014 Significance-Based Computing for Reliability and Power Optimization. Talk at Aristotle University of Thessaloniki, GR.

01.2014 SCoRPiO: Significance Based Computing for Reliability and Power Optimization. Invited Poster at the Workshop on Energy Efficient Electronics and Applications (WEEE). Lausanne, Switzerland.

05.2012 Massively Parallel Programming Models Used as Hardware Description Languages: The OpenCL Case. Invited Talk at University of Toronto, Toronto, ON.

03.2012 Massively Parallel Programming Models Used as Hardware Description Languages: The OpenCL Case. Invited Talk at Aristotle University of Thessaloniki, GR.

10.2011 Massively Parallel Programming Models Used as Hardware Description Languages: The OpenCL Case. Invited Talk at Ecole Polytechnique Fédérale de Lausanne (EPFL).

10.2011 Reliable computing on faulty substrates: a preliminary study. Invited Talk at Ecole Polytechnique Fédérale de Lausanne (EPFL).

08.2011 Massively Parallel Programming Models Used as Hardware Description Languages: The OpenCL Case. Invited Talk at Stanford Research Institute (SRI), Princeton, NJ.

03.2007 Automatic Generation of Streaming Accelerators from a High Level Representation. Invited Talk at the Department of Electrical Engineering, University of California at Riverside, CA.

09.2006 Programming models and Architectures for Reconfigurable Platforms. Invited Talk at Motorola

Software, Systems, Simulation (S3) Symposium, Itasca, IL

03.2006 Programming Models and Architectures for FPGAs. Motorola Symposium on Innovations in DSP and Embedded Systems Design using FPGAs, Schaumburg, IL

09.2005 Automatic Generation of Imaging Architectures from an Algorithmic Representation. Motorola Software, Systems, Simulation (S3) Symposium, Itasca, IL

06.2003 Imaging Technologies at Motorola Labs. Invited Talk at the Computer Engineering and Informatics Department (CEID), University of Patras, Greece

02.2000 Loop-Cache: An Instruction Hierarchy Component for Reduced Energy Consumption". Invited Talk at the Department of Electrical and Computer Engineering, Northwestern University, Evanston, IL

09.1999 Architectural and Compiler Techniques for Energy Reduction in High Performance Processors. Invited Talk at the Department of Electrical and Computer Engineering, Purdue University, W. Lafayette, IN

12.1998 Architectural and Compiler Techniques for Energy Reduction in High Performance Processors. Talk at IBM Research, Austin, TX

11.1998 Architectural and Compiler Techniques for Energy Reduction in High Performance Processors. Talk at Microprocessor Research Labs, Intel Corp. Portland, OR

08.1996 Novel techniques for Power reduction in High Performance Processors. Design Technology Labs, Intel Corp., Santa Clara, CA

Awards and Honors

06.2014 Best paper award nominee, IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP).

06.2000 IEEE Transactions on VLSI. Special issue on the most significant advances in techniques and methodologies for power-conscious design.

11.1992 First Rank, Commencement ceremony of School of Engineering, University of Patras, Greece

1988-1992 Greek Scholarship Foundation academic excellence awards for being in the top 5 in the Department of Computer Engineering and Informatics

Service

Committee and Editorial Services

General Chair/Organizer	WAPCO(17,16,15), ECVW(09)
Program Chair	ECVW (08)
Technical Program Committee	CCGrid(20), DATE(20), DAC(19,18,17), ARC(19,18), EUC(13,12), FPL(11), MICRO(07), ECVW(09,08,07)
Guest Editor	Journal on Computer Vision and Image Understanding. Special issue on embedded computer vision (10)
Publications Chair	MICRO(07)

Workshops Chair FPL(11)

Reviewer

ACM TODAES, ACM TACO, ACM TRTS, ACM TOMCCAP, IEEE Micro, IEEE TCOMP, IEEE TVLSI, IEEE TCAD, IEEE TETC, IEEE TSUSC, Springer JSPS, Elsevier SUSCOM, Elsevier Parallel Computing, Elsevier JPDC, MICRO, FPL, CCGrid, Supercomputing, ICS, ISLPED, ISCA, DAC, DATE, ECVW, ARC, HPDC, ISC, UbiComp, SRDS, WAPCO, Motorola Labs Patent Committee

Professional Associations

1. IEEE Member
2. Member of the European Network of Excellence on High Performance and Embedded Architecture and Compilation (HiPEAC)
3. Member of Technical Chamber of Greece

Departmental Services

1. Director of the Graduate MSc Program of ECE Department at UTH (2018-now)
2. Member of the Graduate MSc committee of ECE Department at UTH (2014-now)
3. Member of the Graduate PhD committee of ECE Department at UTH (2016-now)
4. Member of the Undergraduate Curriculum Committee of ECE Department at UTH (2019)

PhD Supervision

Primary supervisor

1. **Alexandros Patras** - ECE Department, University of Thessaly. Dissertation area: Machine Learning techniques to improve execution flow. *After October 2019.*
2. **Maria-Rafaela Gkeka** - ECE Department, University of Thessaly. Dissertation area: Compiler Techniques for Next Generation 3D Graphics and Compute APIs. *In progress.*
3. **Konstantinos Parasyris** - ECE Department, University of Thessaly. Dissertation area: System software techniques to enhance reliability of modern platforms. (PhD 10.2018). Now researcher at Barcelona Supercomputing Center (BSC).
4. **Muhsen Owaida** - ECE Department, University of Thessaly. Dissertation area: Architectural Synthesis using Parallel Programming Models (PhD 09.2012). Now postdoc at ETH Zurich.

Member of PhD committee

1. **Alexandros Koumbaroulis** - ECE Department, University of Thessaly. Dissertation area: Audio Visual Speech Processing in the Wild. *In progress.*
2. **Panagiotis Koutsovasilis** - ECE Department, University of Thessaly. Dissertation area: Virtual Machine Policies for Improving Energy Efficiency. *In progress.*
3. **Emmanuel Maroudas** - ECE Department, University of Thessaly. Dissertation area: Fault-tolerant Virtual Machine Support on Unreliable Platforms. *In progress.*
4. **Christos Kalogirou** - ECE Department, University of Thessaly. Dissertation area: Software Policies and Mechanisms for Improving Performance and Lowering Power Consumption for the Memory Subsystem of High Performance Computers. *In progress.*
5. **Emmanuel Koutsoumbelias** - ECE Department, University of Thessaly. Dissertation area: Programming and Testing Support for Drone Based Applications (PhD 09.2018).
6. **Vassilis Vassiliadis** - ECE Department, University of Thessaly. Dissertation area: Optimization of Program Execution Using Computational Significance (PhD 11.2017).

7. **George Georgakoudis** - ECE Department, University of Thessaly. Dissertation area: Scheduling and Performance Characterization on Heterogeneous Computing Systems (PhD 05.2016).
8. **Nikolaos A. Foutris** – Department of Informatics and Telecommunications, University of Athens. Dissertation area: Architectures for Dependable Modern Microprocessors (PhD 02.2016).
9. **Antonios S. Nikitakis** – Department of Electronic and Computer Engineering, Technical University of Crete. Dissertation area: High Performance Low Power Embedded Vision Systems (PhD 10.2013).
10. **Georgios Kornaros** – Department of Electronic and Computer Engineering, Technical University of Crete. Dissertation area: Real Time ASIC Monitoring for System-Level Power and Thermal Management (PhD 09.2013).
11. **Ioannis Mavroidis** – Department of Electronic and Computer Engineering, Technical University of Crete. Dissertation area: Algorithm Mapping to Reconfigurable Systems and Systems with Multiple Embedded Processors (PhD 12.2011).
12. **Dimitrios Syrivelis** - ECE Department, University of Thessaly. Dissertation area: Exploiting Reconfigurable Heterogeneous Parallel Architectures in a Multitasking Context: A systems Approach (PhD 06.2009).
13. **Dimitrios Bountas** - ECE Department, University of Thessaly. Dissertation area: EDA tools for Power and Reliability Estimation of ICs (PhD 06.2009).
14. **Dimitrios Karampatzakis** - ECE Department, University of Thessaly. Dissertation area: Reliable ICs (PhD 06.2009).
15. **Somsubhra Mondal** - ECE Department, Northwestern University. Dissertation area: Architectural Optimizations and CAD Tools for Improved Energy Efficiency and Faster Design Closure for FPGAs (PhD 06.2007).

MSc Supervision

1. **Maria Rafaela Gkeka** - ECE Department, University of Thessaly. Dissertation area: Simultaneous Localization and Mapping (SLAM) using the Vulkan Programming Model. *In progress.*
2. **Konstantinos Parasyris** - ECE Department, University of Thessaly. Dissertation area: System software techniques to enhance reliability of modern platforms (MSc July 2017).
3. **George Delis** - ECE Department, University of Thessaly. Dissertation area: Implementation of a Mobile Wireless Sensor Node for the Replacement of Failed Nodes (MSc March 2014).
4. **Konstantis Daloukas** - ECE Department, University of Thessaly. Dissertation area: Compiler and Run-Time Support for OpenCL on Hardware- and Software-Managed Cache Multicores (MSc July 2010).

Citation Metrics (Google Scholar)

Citations: 1463, h-index: 20, i-10 index: 34

Research Funding

1. **Project Title:** Very Low Power GPUs for Mobile Robotics and Virtual Reality (vipGPU)
   Role: Scientific Coordinator. Main author of the proposal.
   Source of funding: Greek General Secretariat for Research and Technology, "Competitiveness, Entrepreneurship and Innovation" Operational Programme.
   Budget and dates: Total project budget 1 million €. Budget share 260,000 €. 2018-2021

2. **Project Title:** A Universal Micro-Server Ecosystem by Exceeding the Energy and Performance Scaling Boundaries (UniServer).
   Role: co-Investigator. One of the authors of the proposal.
   Source of funding: Low power computing, H2020-ICT-2015
   Budget and dates: Total project budget 4.8 million €. Budget share 480,250 €. 2016-2019

3. **Project Title:** Significance-Based Computing for Reliability and Power Optimization (SCoRPiO).
   Role: Coordinator. Main author of the proposal.
   Source of funding: FET-Open Programme, FP7-ICT-2011-C
   Budget and dates: Total budget 1.9 million €. Budget share 420,000 €. 2013-2016

4. **Project Title:** System Software for Future, Heterogeneous, Accelerator-Based Systems (Centaurus)
   Role: co-Investigator. One of the authors of the proposal.
   Source of funding: Greek Ministry of Education, Lifelong Learning and Religious Affairs, Aristeia II Program
   Budget and dates: Total budget 250,000 €, July 2014–November 2015

5. **Project Title:** Advanced Mathematical Methods and Software Platform for solving Multiphysics, Multi-Domain Problems on Modern Computer Architectures: Application to Environmental Engineering and Medical Problems (MATENVMED).
   Role: co-Investigator. One of the authors of the proposal.
   Source of funding: Greek Ministry of Education, Lifelong Learning and Religious Affairs, Thales Program, grant ID: 137
   Budget and dates: Total budget 600,000 €, July 2012–November 2015

6. **Project Title:** Automatic Hardware Generation Using the Streaming Paradigm**.**
   Role: Coordinator. Main author of the proposal.
   Source of funding: Marie Curie International Reintegration Grant (IRG), FP7
   Budget and dates: 100,000 € (November 2008-November 2012)

7. **Project Title:** Low Power Microprocessor Design
   Role: Coordinator. Main author of the proposal.
   Source of funding: Intel Corp.
   Budget and dates: $45,000 per year for 3 years (1996-1998)

Teaching

Course instruction

Fall19-Fall13	Computer Organization and Design (ECE232). University of Thessaly. 2nd year class.
Spr13-Spr09	Introduction to Computer Systems (ECE134). University of Thessaly. 1st year class.
Spr19 – Spr13, Fall11-Fall08	Parallel Computer Architecture (ECE431). University of Thessaly. 4th year class.
Spr19-Spr08	Embedded Systems (ECE435). University of Thessaly. 3rd year class.
Fall18-Fall07	Advanced Topics in Computer Architecture (ECE658). University of Thessaly. Graduate class.

Curriculum development

Computer Organization and Design (ECE232) Major revision

Parallel Computer Architecture (ECE431)	Developed from the beginning
Embedded Systems (ECE435)	Developed from the beginning. Emphasis on FPGA-based MPSoCs
Advanced Topics in Computer Architecture (ECE658)	Developed from the beginning
Advanced Topics in Computer Architecture (Northwestern University)	Developed from the beginning. Graduate course in collaboration with professor Gokhan Memik at Northwestern University.