NESTOR EVMORFOPOULOS

Assistant Professor

University of Thessaly

Dept. of Electrical and Computer Engineering

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EDUCATION

- **National Technical University of Athens (NTUA)**
  PhD. Degree (01/2003)

- **NTUA – University of Athens – University of Piraeus**
  MSc. Degree in Engineering-Economic Systems (06/2001)

- **National Technical University of Athens (NTUA)**
  B.E. Degree in Electrical and Computer Engineering (09/1995)

TEACHING – ACADEMIC EXPERIENCE

- **12/2019 – 05/2020 Univ. of Minnesota (Dept. of Electrical & Computer Engineering)**
  Visiting Scholar
  Research collaboration, under the auspices of the **Fulbright** Foundation, on methods for simulation and order reduction of large-scale circuits and networks based on graph-theoretic concepts
- **01/2013 – present Univ. of Thessaly (Dept. of Electrical & Computer Engineering)**
  Assistant Professor
  Instructor for Courses:
  - Introduction to Electronics
  - Electromagnetic Fields
  - Circuit Simulation Algorithms
  - Computational Methods in Electromagnetics (Electromagnetic Fields II)
- **04/2008 – 12/2012 Univ. of Thessaly (Dept. of Computer & Communication Engineering)**
  Lecturer
  Instructor for Courses:
  - Digital Electronics
  - Electromagnetic Fields
  - Circuit Simulation Algorithms
  - Microprocessor Circuit Design
  - Design of CAD Tools
  - Physics I
  - Physics II

- **03/2003 – 03/2008 Univ. of Thessaly (Dept. of Computer & Communication Engineering)**

  Adjunct Lecturer

  Instructor for Courses:
  - Introduction to Computer Systems
  - Digital Design II with CAD
  - Microprocessor Circuit Design

  Participation in the Teaching of Courses:
  - VLSI Systems Design
  - Embedded Systems
- **02/1996 – 06/2000 NTUA (Dept. of Electrical & Computer Engineering)**

  Teaching Assistant

  Participation in the Teaching of Courses:
  - Digital Systems Laboratory
  - Electronics Laboratory
  - Analog Electronic Systems Laboratory

PARTICIPATION IN R&D PROJECTS

- **05/2013 – 05/2016 SYNERGASIA 11SYN-5-719**
  - Funding agency: General Secretariat of Research and Technology (Greece)
  - Contractors: University of Thessaly – Aristotle Univ. of Thessaloniki – HELIC S.A.
  - Subject: Continuous transistor sizing toolset for nanoscale IC optimization
- **06/2005 – 06/2008 PENED 03ED**
  - Funding agency: General Secretariat of Research and Technology (Greece)
  - Contractors: University of Thessaly – HELIC S.A.
  - Subject: Optimal sizing of transistors and power distribution wires in ICs
- **09/2002 – 09/2005 "New methods of leakage power analysis in ICs"**
  - Funding agency: Intel Corp. (USA)
  - Contractor: University of Thessaly
- **06/1998 – 06/2002 "New approaches to sample-based maximum estimation"**
  - Funding agency: Intel Corp. (USA)
  - Contractor: National Technical University of Athens
- **08/1998 – 08/1999 PEP**
  - Funding agency: Greek Ministry of Development
  - Contractors: National Technical University of Athens – KNAUF
  - Subject: Development of real-time statistical quality control techniques
- **02/1998 – 02/2000 PAVE96**
  - Funding agency: General Secretariat of Research and Technology (Greece)
  - Contractors: National Technical University of Athens – ELBISCO
  - Subject: Development of real-time statistical quality control techniques
- **06/1997 – 02/1998 "Development of electronic smart tag prototypes"**
  - Funding agency: Hellenic Society for the Protection of Intellectual Property
  - Contractor: National Technical University of Athens

- **10/1996 – 10/1998 ESPRIT-III (Technologies for components and subsystems)**
  - Funding agency: European Union
  - Contractors: National Technical University of Athens – INTRACOM S.A.
  - Subject: Design and fabrication of mixed-signal ASICs in 0.7μm CMOS process
- **12/1994 – 10/1995 "Design of active bandpass filters of military specifications"**
  - Funding agency: Hellenic Aerospace Industry
  - Contractor: National Technical University of Athens

PUBLICATIONS

- **Book Chapters**

1. N. Evmorfopoulos, S. Bantas, and G. Stamoulis, "Simulation techniques for large-scale circuits", in T. Noulis and M. Soma (eds.), *Mixed-Signal Circuits*, CRC Press, 2016 (**Invited**).

- **Publications in International Journals**

2. N. Evmorfopoulos, G. Floros, C. Antoniadis, and G. Stamoulis, "A survey of recent advances in model order reduction for large-scale VLSI interconnects", *Integration, The VLSI Journal*, to appear, 2020 (**Invited**).

3. G. Floros, N. Evmorfopoulos, and G. Stamoulis, "Efficient IC hotspot thermal analysis via low-rank model order reduction", *Integration, The VLSI Journal*, vol. 66, pp. 1-8, 2019 (**Invited**).

4. G. Floros, K. Daloukas, N. Evmorfopoulos, and G. Stamoulis, "A preconditioned iterative approach for efficient full chip thermal analysis on massively parallel platforms", *Technologies*, vol. 7, no. 1, 2019 (**Invited**).

5. K. Daloukas, N. Evmorfopoulos, P. Tsompanopoulou, and G. Stamoulis, "Fast transform-based preconditioners for large-scale power grid analysis on Graphics Processing Units (GPUs)", *IEEE Trans. Computer-Aided Design*, vol. 35, no. 10, pp. 1653-1666, 2016.

6. N. Evmorfopoulos, D. Karampatzakis, and G. Stamoulis, "Accurate minimum area design of power/ground meshes subject to voltage drop constraints", *Journal of Active and Passive Electronic Devices*, vol. 2, no. 1, pp. 55-70, 2007.

7. N. Evmorfopoulos, G. Stamoulis, and J. Avaritsiotis, "A Monte Carlo approach for maximum power estimation based on extreme value theory", *IEEE Trans. Computer-Aided Design*, vol. 21, no. 4, pp. 415-432, 2002.

8. N. Evmorfopoulos and J. Avaritsiotis, "An adaptive digital fuzzy architecture for application-specific integrated circuits", *Active and Passive Electronic Components*, vol. 25, no. 4, pp. 289-306, 2002.

9. N. Evmorfopoulos and J. Avaritsiotis, "A new statistical method for maximum power estimation in CMOS VLSI circuits", *Active and Passive Electronic Components*, vol. 22, no. 3, pp. 215-233, 2000.

- **Publications in Proceedings of International Conferences**

10. C. Antoniadis, M. Mihajlovic, N. Evmorfopoulos, G. Stamoulis, and V. Pavlidis, "Efficient linear system solution techniques in the simulation of large dense mutually inductive circuits", *IEEE Int. Conf. Computer Design* (*ICCD*), Abu Dhabi, United Arab Emirates, 2019.

11. G. Floros, C. Chatzigeorgiou, N. Evmorfopoulos, and G. Stamoulis, "THANOS: Eliminating redundant states in transient thermal analysis", *IEEE Int. Workshop on Thermal Investigations of ICs and Systems* (*THERMINIC*), Lecco, Italy, 2019.

12. D. Garyfallou, C. Antoniadis, N. Evmorfopoulos, and G. Stamoulis, "A sparsity-aware MOR methodology for fast and accurate timing analysis of VLSI interconnects", *IEEE Int. Conf. Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design* (*SMACD*), Lausanne, Switzerland, 2019.

13. G. Floros, N. Evmorfopoulos, and G. Stamoulis, "Efficient circuit reduction in limited frequency windows", *IEEE Int. Conf. Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design* (*SMACD*), Lausanne, Switzerland, 2019.

14. C. Antoniadis, N. Evmorfopoulos, and G. Stamoulis, “A rigorous approach for the sparsification of dense matrices from model order reduction of high frequency circuits”, *IEEE/ACM Design Automation Conf.* (*DAC*), Las Vegas, USA, 2019.

15. C. Antoniadis, N. Evmorfopoulos, and G. Stamoulis, “Efficient sparsification of dense circuit matrices in model order reduction”, *IEEE/ACM Asia and South Pacific Design Automation Conf.* (*ASP-DAC*), Tokyo, Japan, 2019.

16. G. Paliaroutis, P. Tsoumanis, N. Evmorfopoulos, G. Dimitriou, and G. Stamoulis, “Multiple transient faults in combinational logic with placement considerations”, *IEEE Int. Conf. Modern Circuits and Systems Technologies* (*MOCAST*), Thessaloniki, Greece, 2019 (**Nominated for Best Paper Award**).

17. G. Floros, N. Evmorfopoulos, and G. Stamoulis, “Efficient hotspot thermal simulation via low-rank model order reduction”, *IEEE Int. Conf. Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design* (*SMACD*), Prague, Czech Republic, 2018 (**Nominated for Best Paper Award**).

18. C. Antoniadis, N. Evmorfopoulos, and G. Stamoulis, “On the sparsification of the reluctance matrix in RLCK circuit transient analysis”, *IEEE Int. Conf. Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design* (*SMACD*), Prague, Czech Republic, 2018.

19. D. Garyfallou, N. Evmorfopoulos, and G. Stamoulis, “A combinatorial multigrid preconditioned iterative method for large scale circuit simulation on GPUs”, *IEEE Int. Conf. Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design* (*SMACD*), Prague, Czech Republic, 2018.

20. G. Paliaroutis, P. Tsoumanis, N. Evmorfopoulos, G. Dimitriou, and G. Stamoulis, “A placement aware soft error rate estimation of combinational circuits for multiple transient faults in CMOS technology”, *IEEE Int. Symp. Defect and Fault Tolerance in VLSI and Nanotechology Systems* (*DFT*), Chicago, USA, 2018.

21. C. Antoniadis, D. Garyfallou, N. Evmorfopoulos, and G. Stamoulis, “EVT-based worst case delay estimation under process variation”, *IEEE/ACM Design, Automation & Test in Europe* (*DATE*), Dresden, Germany, 2018.

22. M. Tsiampas, N. Evmorfopoulos, K. Daloukas, J. Moondanos, and G. Stamoulis, “A power-supply noise aware dynamic timing analysis methodology, based on a statistical prediction engine”, *IEEE Int. Conf. Design and Technology of Integrated Systems in Nanoscale Era* (*DTIS*), Taormina, Italy, 2018.

23. G. Floros, K. Daloukas, N. Evmorfopoulos, and G. Stamoulis, “A parallel iterative approach for efficient full-chip thermal analysis”, *IEEE Int. Conf. Modern Circuits and Systems Technologies* (*MOCAST*), Thessaloniki, Greece, 2018 (**Best Paper Award**).

24. D. Garyfallou, N. Evmorfopoulos, and G. Stamoulis, “Large-scale circuit simulation exploiting combinatorial multigrid on massively parallel architectures”, *IEEE Int. Conf. Modern Circuits and Systems Technologies* (*MOCAST*), Thessaloniki, Greece, 2018.

25. G. Paliaroutis, P. Tsoumanis, N. Evmorfopoulos, G. Dimitriou, and G. Stamoulis, “Placement-based SER estimation in the presence of multiple faults in combinational logic”, *IEEE Int. Symp. Power and Timing Modeling, Optimization and Simulation* (*PATMOS*), Thessaloniki, Greece, 2017.

26. C. Antoniadis, G. Karakonstantis, N. Evmorfopoulos, A. Burg, and G. Stamoulis, “On the statistical memory architecture exploration and optimization”, *IEEE/ACM Design, Automation & Test in Europe* (*DATE*), Grenoble, France, 2015.

27. D. Ntioudis, C. Kalonakis, P. Giannakou, C. Antoniadis, G. Stamoulis, P. Tsompanopoulou, N. Evmorfopoulos, J. Moondanos, and G. Dimitriou, “CCSOpt: A continuous gate-level resizing tool”, *IEEE Int. Conf. Modern Circuits and Systems Technologies* (*MOCAST*), Thessaloniki, Greece, 2015.

28. P. Giannakou, C. Antoniadis, C. Kalonakis, D. Ntioudis, G. Stamoulis, P. Tsompanopoulou, N. Evmorfopoulos, J. Moondanos, and G. Dimitriou, “GDS2trim: Physical layout manipulation utility for continuous transistor sizing”, *IEEE Int. Conf. Modern Circuits and Systems Technologies* (*MOCAST*), Thessaloniki, Greece, 2015.

29. T. Strousidou, C. Antoniadis, I. Arvanitakis, G. Dimitriou, N. Evmorfopoulos, P. Tsompanopoulou, P. Bozanis, and G. Stamoulis, “Accelerating GORDIAN-based placement

through null-space removal techniques", *Panhellenic Conf. on Electronics and Telecommunications* (*PACET*), Ioannina, Greece, 2015.

30. I. Apostolopoulou, K. Daloukas, N. Evmorfopoulos, and G. Stamoulis, "Selective inversion of inductance matrix for large-scale sparse RLC simulation", *IEEE/ACM Design Automation Conf.* (*DAC*), San Francisco, USA, 2014.

31. K. Daloukas, N. Evmorfopoulos, P. Tsompanopoulou, and G. Stamoulis, "A 3-D fast transform-based preconditioning approach for large-scale power grid analysis on massively parallel architectures", *IEEE/ACM Int. Symp. Quality Electronic Design* (*ISQED*), Santa Clara, USA, 2014.

32. S. Ioannidis, D. Ntioudis, C. Antoniadis, A. Dadaliaris, P. Tsompanopoulou, N. Evmorfopoulos, and G. Stamoulis, "Optimization of an integrated circuit placement algorithm in a parallel environment", *Int. Conf. Computer Science, Computer Engineering, and Social Media* (*CSCESM*), Thessaloniki, Greece, 2014.

33. K. Daloukas, A. Marnari, N. Evmorfopoulos, P. Tsompanopoulou, and G. Stamoulis, "A parallel fast transform-based preconditioning approach for electrical-thermal co-simulation of power delivery networks", *IEEE/ACM Design, Automation & Test in Europe* (*DATE*), Grenoble, France, 2013.

34. A. Cevrero, N. Evmorfopoulos, C. Antoniadis, P. Ienne, Y. Leblebici, A. Burg, and G. Stamoulis, "Fast and accurate BER estimation methodology for I/O links based on extreme value theory", *IEEE/ACM Design, Automation & Test in Europe* (*DATE*), Grenoble, France, 2013.

35. K. Daloukas, N. Evmorfopoulos, G. Drasidis, M. Tsiampas, P. Tsompanopoulou, and G. Stamoulis, "Fast transform-based preconditioners for large-scale power grid analysis on massively parallel architectures", *IEEE/ACM Int. Conf. Computer-Aided Design* (*ICCAD*), San Jose, USA, 2012 (**Nominated for "William J. McCalla" Best Paper Award**).

36. N. Evmorfopoulos, M. Rammou, G. Stamoulis, and J. Moondanos, "Characterization of the worst-case current waveform excitations in general RLC-model power grid analysis", *IEEE/ACM Int. Conf. Computer-Aided Design* (*ICCAD*), San Jose, USA, 2010.

37. M. Tsiampas, D. Bountas, P. Merakos, N. Evmorfopoulos, S. Bantas, and G. Stamoulis, "A power grid analysis and verification tool based on a statistical prediction engine", *IEEE Int. Conf. Electronics, Circuits and Systems* (*ICECS*), Athens, Greece, 2010.

38. D. Bountas, N. Evmorfopoulos, and G. Stamoulis, "A macromodel technique for VLSI dynamic simulation by mapping pre-characterized transitions", *IEEE Int. Conf. Computer Design* (*ICCD*), Lake Tahoe, USA, 2008.

39. D. Karampatzakis, M. Tsiampas, N. Evmorfopoulos, and G. Stamoulis, "A design flow for the precise identification of the worst-case voltage drop in power grid analyses", *Panhellenic Conf. on Informatics* (*PCI*), Samos, Greece, 2008.

40. N. Evmorfopoulos, D. Karampatzakis, and G. Stamoulis, "Precise identification of the worst-case voltage drop conditions in power grid verification", *IEEE/ACM Int. Conf. Computer-Aided Design* (*ICCAD*), San Jose, USA, 2006.

41. D. Karampatzakis, N. Evmorfopoulos, M. Tsiampas, and G. Stamoulis, "An RTL-to-grid design flow for power grid verification based on a statistical estimation engine", *IEEE PRIME*, Lecce, Italy, 2006.

42. D. Karampatzakis, N. Evmorfopoulos, and G. Stamoulis, "A statistically-based engine for P/G network optimization", *IEEE PRIME*, Lausanne, Switzerland, 2005.

43. N. Evmorfopoulos, D. Karampatzakis, and G. Stamoulis, "Voltage-drop-constrained optimization of power distribution network based on reliable maximum current estimates", *IEEE/ACM Int. Conf. Computer-Aided Design* (*ICCAD*), San Jose, USA, 2004.

44. N. Evmorfopoulos and J. Avaritsiotis, "Adaptive digital fuzzy hardware in application-specific integrated circuits", *IEEE Int. Conf. Electronics, Circuits and Systems* (*ICECS*), Paphos, Cyprus, 1999.

- **Publications in International Collective Volumes**

45. N. Evmorfopoulos, J. Avaritsiotis, and G. Stamoulis, "Maximum power estimation in CMOS VLSI circuits", in A. Nassiopoulou and X. Zanni (eds.), *Microelectronics, Microsystems and Nanotechnology*, World Scientific, 2001.

- **Poster Presentations in International Conferences**

46. G. Floros, N. Evmorfopoulos, and G. Stamoulis, “Efficient reduction of large circuit models over limited frequency windows”, *IEEE/ACM Design Automation Conf.* (*DAC*), Las Vegas, USA, 2019.

47. K. Daloukas, N. Evmorfopoulos, P. Tsompanopoulou, and G. Stamoulis, “Fast transform-based solvers as parallel preconditioners for large-scale power grid analysis on massively parallel architectures”, *IEEE/ACM Design Automation Conf.* (*DAC*), San Francisco, USA, 2012.

48. K. Daloukas, M. Rammou, G. Drasidis, M. Tsiampas, N. Evmorfopoulos, P. Tsompanopoulou, and G. Stamoulis, “Parallel preconditioners based on fast Poisson solvers for efficient large-scale power grid analysis”, *IEEE/ACM Design Automation Conf.* (*DAC*), San Francisco, USA, 2012.

49. D. Karampatzakis, N. Evmorfopoulos, and G. Stamoulis, “I-Xtreme: A statistically-based engine for P/G network optimization”, *IEEE/ACM Design Automation Conf.* (*DAC*), Anaheim, USA, 2005.

- **Patents**

50. K. Daloukas and N. Evmorfopoulos, “Iterative solution using compressed inductive matrix for efficient simulation of very large scale circuits”, *U.S. patent no. 9959377 B2*, 2018.

51. K. Daloukas, N. Evmorfopoulos, P. Tsompanopoulou, and G. Stamoulis, “Large-scale power grid analysis on parallel architectures”, *U.S. patent no. 9858369 B2*, 2018.

52. G. Stamoulis, S. Bantas, D. Bountas, N. Evmorfopoulos, M. Tsiampas, and P. Merakos, “System and method for determining simulated response extrema for integrated circuit power supply networks”, *U.S. patent no. 8516423 B2*, 2013.

53. G. Stamoulis, S. Bantas, D. Bountas, N. Evmorfopoulos, M. Tsiampas, and P. Merakos, “System and method for fast power grid and substrate noise simulation”, *U.S. patent app. no. 0016652 A1*, 2012.

- **Technical reports**

54. N. Evmorfopoulos, “Some results on diagonally dominant matrices with positive diagonal elements”, *Univ. of Thessaly tech. rep. TR-09-09-001*, 2010.

CITATIONS

- 100+ cross-citations

INVITED SPEECHES

- “Complexity in large-scale circuit simulation”, *24th Summer School – Conference on Dynamical Systems and Complexity*, Volos, 2017.
- “Large-scale circuit simulation”, *Design Test Verification and EDA Workshop* (*DTVEDA*), Volos, 2017.
- “Simulation of large-scale circuits and circuit models”, *IEEE Student Branch Workshop*, Volos, 2016.

DISTINCTIONS

- Award from the Fulbright Foundation for conducting research in the USA as Visiting Scholar for the academic year 2019-2020.
- Nomination for the “William J. McCalla” Best Paper Award at the *IEEE/ACM International Conference on Computer-Aided Design* (*ICCAD*), 2012.

- Best Paper Award at the *IEEE Int. Conf. Modern Circuits and Systems Technologies* (*MOCAST*), 2018.
- Nomination for Best Paper Award at the *IEEE Int. Conf. Modern Circuits and Systems Technologies* (*MOCAST*), 2019.
- Nomination for Best Paper Award at the *IEEE Int. Conf. Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design* (*SMACD*), 2018.
- Award from Helic S.A. for contribution in the corporate paper entitled "A high-capacity power integrity flow supporting inductive rail effects with transistor-level accuracy", which received the Best Paper Award at the *Magma Users Summit on Integrated Circuits* (*MUSIC*), 2010.
- Grant by Intel Corp. (USA) for PhD. research.
- Scholarship award in the MSc. program of the National Technical University of Athens.

OTHER ACTIVITIES

- Supervisor in 2 completed PhD theses and 5 ongoing PhD theses.
- Supervisor in over 25 master theses and over 100 diploma theses.
- Special Sessions Chair for the *Panhellenic Conference on Electronics and Telecommunications* (*PACET*) 2019.
- Member of the Program Committee for the *IEEE International Conference on Modern Circuits and Systems Technologies* (*MOCAST*) 2016-2019.
- Reviewer for the following international journals and conferences:
  - IEEE Transactions on Computer-Aided Design
  - IEEE Transactions on VLSI Systems
  - International Journal of RF and Microwave Computer-Aided Engineering (RFMiCAE)
  - IEEE/ACM International Conference on Computer-Aided Design (ICCAD)
  - IEEE/ACM Design Automation Conference (DAC)
  - IEEE/ACM Asia and South-Pacific Design Automation Conference (ASP-DAC)
  - IEEE/ACM Design, Automation & Test in Europe (DATE)
  - IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)
  - International Conference of Numerical Analysis and Applied Mathematics (ICNAAM)
  - Panhellenic Conference on Informatics (PCI)
- Member of the committee for graduate studies at the Dept. of Computer and Communication Engineering of the University of Thessaly (2009-2011).
- Member of the library committee of the University of Thessaly (2008-2012).
- Member of the committee for evaluation of University scholars at the Dept. of Electrical and Computer Engineering of the University of Thessaly (2014-2017).
- Member of the committee for graduate studies at the Dept. of Electrical and Computer Engineering of the University of Thessaly (2017-present).
- Longtime collaboration with Helic S.A. (part of Ansys Inc. since 2018) as scientific consultant in topics involving CAD/EDA tools and circuit simulation. Key points in this collaboration are: (a) the successful completion of 2 joint funded projects, (b) the filing of 3 joint US patents, (c) the hiring of 4 former undergraduate/graduate students and 1 postdoctoral fellow by the company.
- Participation in the founding of a startup company (Nanotropic S.A., 2008).
- Member of the Institute of Electrical and Electronics Engineers (IEEE) since 1995.